REMARKS

Claims 2 and 4 through 19 are now pending in this application. Claims 2, 3 and 7 through 11 have been allowed. Claims 12 through 19 stand withdrawn. In response to the non-final Office Action dated March 27, 2006, claims 1 and 3 have been cancelled. A petition for one month extension of the period for response, with appropriate fee charge authorization, is filed herewith. Favorable reconsideration of the application is respectfully solicited.

The rejections of claims 1 and 3 in the Office Action are now moot, as these claims have been cancelled.

Claims 4 and 6 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent 3,641,450 (Lunn). The rejection is respectfully traversed.

Regarding claim 4, the Office Action reads the claimed elements of Fig. 1 of Lunn as follows. Transistor 106 is read on the first claimed transistor and transistor 107 is read on the second claimed transistor. However, in contrast to the reading in the Office Action, loads 126 and 127 are not connected to transistors 106 and 107. As claim 4 requires that a terminal of the first transistor be connected to the first potential via a load and a terminal of the second transistor be connected to the first potential via a load, the application of Lunn in the Office Action does not anticipate claim 4.

Moreover, claim 4 is not anticipated if the claimed elements are read on any other combination of elements in Lunn. For example, if transistors 101 and 102 are read as first and second transistors of the present invention, transistors 134 and 135 are read as first and second variable impedance devices, and resistors 130 and 131 are read as first and second impedance devices, the potentials at the junction points of transistors 134 and 135 are the same as the potential at node 111 (or the junction point of resistors 130 and 131).

In contrast, in claim 4, the first and second variable impedance devices are connected between third terminals of the first and second transistors, the first and second impedance devices are connected to the third terminals of the first and second transistors, respectively, and the ends of the first and second impedance devices receive the second potential. A resistive element is connected between a junction point between the first and second variable impedance devices and the second potential. Therefore, the potential at the junction point between the first and second variable impedance devices is not the same as the second potential.

For example, in the embodiment of Fig. 13, FETs 11 and 12 are connected between nodes N1 and N2, and resistance 13 is connected between nodes N3 and N13. Therefore, the potential at node N3 is not the same as the potential at node N13.

Regarding claim 6, the first and second variable impedance devices are connected between first and second nodes, the first and second resistive elements are connected between the first and second nodes and third and fourth nodes, respectively, and the third and fourth nodes receive the third and fourth potentials, respectively. A third resistive element is connected between a junction point between the first and second variable impedance devices and a fifth node receiving the fifth potential. Therefore, in contrast to the reading in the Office Action, the potential at the junction point between the first and second variable impedance devices is not the same as the fifth potential.

Accordingly, it is submitted that claims 4 and 6 are not anticipated by Lunn. Withdrawal of the rejection is respectfully solicited.

Allowance of the application is respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in

fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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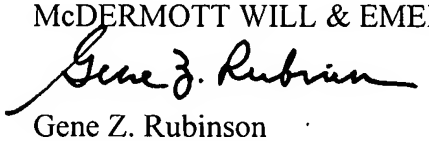

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